Abstract of the Disclosure:

A basic portion layer 21 of a substrate electrode 12a connected to a projecting electrode 13 electrically and mechanically on a substrate member of ceramics. The substrate member on which the basic portion layer 21 is formed is subjected to sintering. A surface of the basic portion layer 21 in the sintered substrate member is polished. On the polished basic portion layer 21, the plating layers 22, 23 are formed, so that surface roughness of the substrate electrode 12a may be, for example, not larger than 0.1 μmRMS. Accordingly, junction strength of an integrated circuit element mounted on a packaging substrate by a flip-chip method can be improved.